CLAIMS

1. Method for processing an input bit sequence in a digital communication system, said method including the steps of:

a) storing (66) the bits of said input bit sequence at locations of a memory means indicated by a first interleaving scheme,

b) converting (69) output bit positions into input bit positions according to an inverse of a second interleaving scheme,

c) reading out (73) bits stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes,

d) processing (74) said interleaved sequence according to further physical processing steps,

wherein the execution periods of the converting and processing steps overlap in time.

2. Method for processing an input bit sequence in a digital communication system, said method including the steps of:

a) storing the bits of said input bit sequence in a

memory means,

b) converting output bit positions into input bit positions according to an inverse of a sequential application of a first interleaving scheme and a second interleaving scheme,

c) reading out bits stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes,

d) processing said interleaved sequence according to further physical processing steps,

wherein the execution periods of the converting and processing steps overlap in time.

3. Method according to claim 1 or 2, wherein the converting and processing steps are executed in essentially the same period of time.

4. Method according to one of the claims 1 to 3, wherein the execution periods of the converting and storing steps overlap in time.

5. Method according to one of the claims 1 to 4, wherein said reading step is adapted to begin with its operations at the earliest possible instant in time after said storing step has finished its operations.

6. Method according to one of the claims 1 to 5, wherein said further physical processing steps include a step of modulation.

7. Method according to one of the claims 1 to 6, wherein said further physical processing steps include a step of spreading.

8. A computer program product directly loadable into the internal memory of a communication unit, comprising software code portions for performing the steps of one of the claims 1 to 7, when the product is run on at least one processor of the communication unit.

9. Apparatus for processing an input bit sequence in a digital communication system, including:

a) a memory means (75) capable of storing said input bit sequence,

b) a first processing unit (76) adapted to store the bits of said input bit sequence at locations of said memory means indicated by a first interleaving scheme,

c) a second processing unit (77, 78) adapted to
- convert output bit positions into input bit positions according to an inverse of a second interleaving scheme,
- read out bits stored at locations of said memory means corresponding to said input bit positions,

thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes,
- process said interleaved sequence according to further physical processing steps,

wherein the second processing unit is adapted to convert bit positions and to process said interleaved sequence in overlapping periods of time.

10. Apparatus for processing an input bit sequence in a digital communication system, including:

a) a memory means capable of storing said input bit sequence,

b) a first processing unit adapted to store the bits of said input bit sequence in said memory means,

c) a second processing unit adapted to
- convert output bit positions into input bit positions according to an inverse of a sequential application of a first interleaving scheme and a second interleaving scheme,
- read out bits stored at locations of said memory means corresponding to said input bit positions, thereby generating an interleaved sequence which is interleaved according to said first and said second interleaving schemes,
- process said interleaved sequence according to further physical processing steps,

wherein the second processing unit is adapted to convert bit positions and to process said interleaved sequence in overlapping periods of time.

11. Apparatus according to claim 9 or 10, wherein the second processing unit is adapted to convert bit positions and to process said interleaved sequence in essentially the same period of time.

12. Apparatus according to one of the claims 9 to 11 adapted to convert bit positions and to store the bits of said input bit sequence in overlapping periods of time.

13. Apparatus according to one of the claims 9 to 12 adapted to begin with reading operations at the earliest possible instant in time after having finished the storing operations.

14. Apparatus according to one of the claims 9 to 13, wherein said further physical processing steps include a step of modulation.

15. Apparatus according to one of the claims 9 to 14, wherein said further physical processing steps include a step of spreading.